REMARKS

In the December 12, 2005 Office Action, the Examiner:

- Rejected claims 1, 3, 4, 6 and 8-11 under 35 U.S.C. 103(a) as unpatentable over Levinson ("*Levinson*", U.S. Pat. No. 5,019,769) in view of Swartz ("*Swartz*", U.S. Pat. No. 6,021,947);
- Rejected claims 12-21, 23-30 and 33-38 under 35 U.S.C. 103(a) as unpatentable over *Levinson*;
- Rejected claims 2 and 5 under 35 U.S.C. 103(a) as unpatentable over *Levinson* in view of *Swartz* as applied to claims 1 and 4, and further in view of Stephenson ("*Stephenson*", U.S. App. No. 2002/0027688); and
- Rejected claim 7 under 35 U.S.C. 103(a) as unpatentable over *Levinson* in view of *Swartz* as applied to claim 4, and further in view of King *et al*,. ("*King*", U.S. Pat. No. 5,812,572).

Applicants have amended the claims by replacing "predefined locations" with "predefined memory mapped locations" and by making a similar change to claim 19. Claims 34 and 38 have also been revised to clarify that the interface enables the host to read digital values from any of the memory mapped locations specifically mentioned in these claims. The rejected claims contain 7 independent claims, namely claims 1, 4, 8, 12, 14, 34, and 38.

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 1, 3, 4, 6 and 8-11 under 35 U.S.C. 103(a) as unpatentable over *Levinson* in view of *Swartz*; rejected claims 12-21, 23-30 and 33-38 under 35 U.S.C. 103(a) as unpatentable over *Levinson*; rejected claims 2 and 5 under 35 U.S.C. 103(a) as unpatentable over *Levinson* in view of *Swartz* as applied to claims 1 and 4, and further in view of *Stephenson*; and rejected claim 7 under 35 U.S.C. 103(a) as unpatentable over *Levinson* in view of *Swartz* as applied to claim 4, and further in view of *King*. To establish a prima facie case of obviousness, three basic criteria must be met, namely:

> 1) There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;

2) There must be a reasonable expectation of success; and

3) The prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure.[1]

The Examiner has rejected claims 1, 3, 4, 6 and 8-11 under 35 U.S.C. 103(a) as unpatentable over *Levinson* in view of *Swartz*, and rejected claims 12-13 under 35 U.S.C. 103(a) as unpatentable over *Levinson*. These claims contain 4 independent claims, namely claims 1, 4, 8, and 12. Both independent claims 1 and 4 contain the following limitation:

> an interface configured to enable a host to read from host-specified locations within the memory, including said predefined memory mapped locations of the memory, so as to obtain one or more of said digital values corresponding to current operating conditions of the optoelectronic transceiver

(Emphasis added).

Independent claim 8 contains the following limitation:

> an interface for allowing a host to read from host specified locations within the memory, including said predefined memory mapped locations of the memory, so as to obtain one or more of said digital values corresponding to current operating conditions of the optoelectronic transceiver

(Emphasis added).

Independent claim 12 contains the following limitation:

> enabling the host device to read from and write to host specified locations within a controller of the optoelectronic transceiver, the host specified locations including a set of predefined memory mapped locations in which are stored digital values corresponding to current operating conditions of the optoelectronic transceiver,

(Emphasis added).

In other words, all of these independent claims require that the host device is able to access host specified locations within the memory, including the predefined memory mapped locations. This allows the host device to read from specific locations within the memory

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[1] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

without having to read an entire diagnostics file from the memory. This has many advantages, including speed of data access, reduction in bandwidth used between the optoelectronic transceiver and the host device, improved efficiency, reduced load and wear on the memory, etc. As will be shown below, this is completely different to the Applicants' *Levinson* patent.

The addition of the term "memory mapped" to qualify "locations" or "addresses" emphasizes that the locations in question are individual locations whose addresses are known (and memory mapped) not only to the controller but also to the host device.

With regard to independent claims 1, 4, and 8 the Examiner states that *Levinson* discloses:

> an interface (including RS232 I10 port 200) configured to enable a host (computer 202) to read from host-specified locations within the memory, including the predefined locations of the memory, so as to obtain one or more of the digital values corresponding to current operating conditions of the optoelectronic transceiver (column 6, lines 40-46; column 15, lines 25-66).

(Emphasis added). Excerpts from the cited portions of *Levinson* state:

> An RS232 input/output port 200 couples the microcontroller 162 to external devices, such an ASCII terminal or desktop computer 202. The computer 202 can read data stored in the EEPROM 166, and can set parameters for the controller 160, . . .
>
> Referring to FIGS. 3 and 11, the controller's software . . . allows the user to access status information in the controller via a host computer 202, to view the data stored in the controller's nonvolatile memory 166, . . .

As can be seen from the above cited portions, *Levinson* only teaches that the host computer can read data stored in memory, but not how the data is read. There is no teaching in *Levinson* that the host computer can access specify memory locations known by the host. Similarly, *Levinson* does not teach memory mapped access by the host computer to data stored in the controller. Further, there is no teaching in *Levinson* about the nature or content of the commands sent by the host computer to the controller, *i.e.*, there is no teaching that the host computer requests data only from specific locations or addresses in memory. Accordingly, *Levinson* does not disclose, teach, or suggest that the host computer can read from host specified locations within the memory, including the specific predefined locations

where the digital values corresponding to current operating conditions of the optoelectronic transceiver are stored.

Furthermore, as *Levinson* is the Applicants' own patent, Applicants can explain how the commercial embodiment of this invention actually operated. In essence, the host computer requested the data from the microcontroller. The microcontroller then sent all of the data stored in memory to the host, *i.e.*, a memory dump. The host did not have the ability to read from host specified locations within the memory. Rather, when the host requested data stored in memory, it received all the data stored in memory irrespective of its specific location in the memory.

Swartz also does not disclose a host device that is able to access host specified locations within the memory including the predefined locations.

Applicant also traverses the Examiner's assertion that storing the specifically identified digital values (temperature, supply voltage, laser bias current, output power, received power), at memory mapped locations - where they can be read by a host device by specifying the same memory mapped locations would be obvious from *Levinson*. The Examiner's correctly points out that *Levinson* teaches monitoring these operating conditions. However, as of the priority date of this application, it was not obvious that it was practical to communicate all of this information to a host device, nor was it obvious that all of this operating condition information could be communicated efficiently to a host device by storing digital values for these operating conditions at memory mapped locations known to the host device. By leaving it up to the host device when to receive this information, and by leaving it up to the host to determine which digital values to read, the present invention circumvents many of the communication and system design issues that made it impractical (in the past) to make so much operating condition information available to a host device. There is simply no teaching in *Levinson*, nor in the other prior art of record, which teaches these ideas.

For the above reasons, independent claims 1, 4, 8, and 12, as well as their dependent claims, are patentable over *Levinson* with or without *Swartz*, as neither of these references

disclose, teach, or suggest that the host device is able to access host specified locations within the memory including the predefined locations.

With regard to independent claims 14, 34, and 38, the Examiner states that *Levinson* teaches:

> an interface (including RS232 110 port 200) configured to enable a host (computer 202) having at least one of the addresses to read from the predefined locations in memory (column 6, lines 40-46; column 15, lines 25-66).

Excerpts from the sections of *Levinson* relied upon by the Examiner can be found in the text quoted above.

Levinson, however, only teaches that "[t]he computer 202 can read data stored in the EEPROM 166." Therefore, for at least the same reasons presented above, independent claims 14, 35, and 38, and their dependant claims, are patentable over *Levinson*, as *Levinson* does not disclose, teach, or suggest that the host can access specific predefined memory mapped locations in the memory.

Furthermore, *Levinson* does not disclose, teach, or suggest that the host has "at least one of the addresses to read from the predefined locations in memory." In fact, the host computer in *Levinson* would not require knowledge of any specific addresses in memory, as it simply requests a memory dump from the microcontroller. Accordingly for this reason alone, independent claims 35 and 38, and their dependant claims, are patentable over *Levinson*, as *Levinson* does not disclose, teach, or suggest that the host accesses predefined memory mapped locations in memory by knowing exactly which addresses in memory to read from.

Based on the above, independent claims 1, 4, 8, 12, 14, 34, and 38, as well as their dependent claims are patentable over the cited prior art references, as these references do not teach or suggest all of the claim limitations.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is now in a condition for allowance. However, should the Examiner believe that the claims are not in condition for allowance, the Applicant encourages the Examiner to call the undersigned attorney at 650-843-7519 to set up an interview.

If there are any fees or credits due in connection with the filing of this Amendment, including any fees required for an Extension of Time under 37 C.F.R. Section 1.136, authorization is given to charge any necessary fees to our Deposit Account No. 50-0310 (order No. 60900-0197-US). A copy of this sheet is enclosed for such purpose.

Respectfully submitted,

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